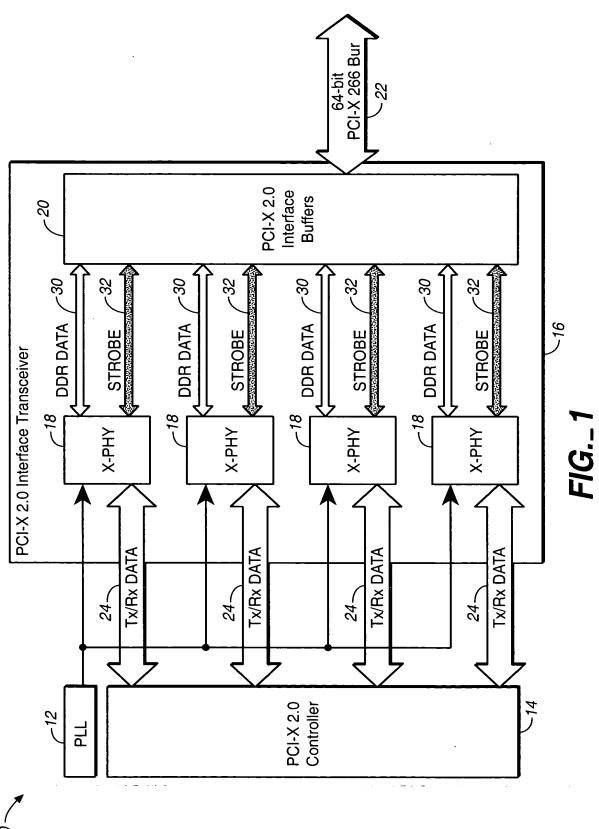
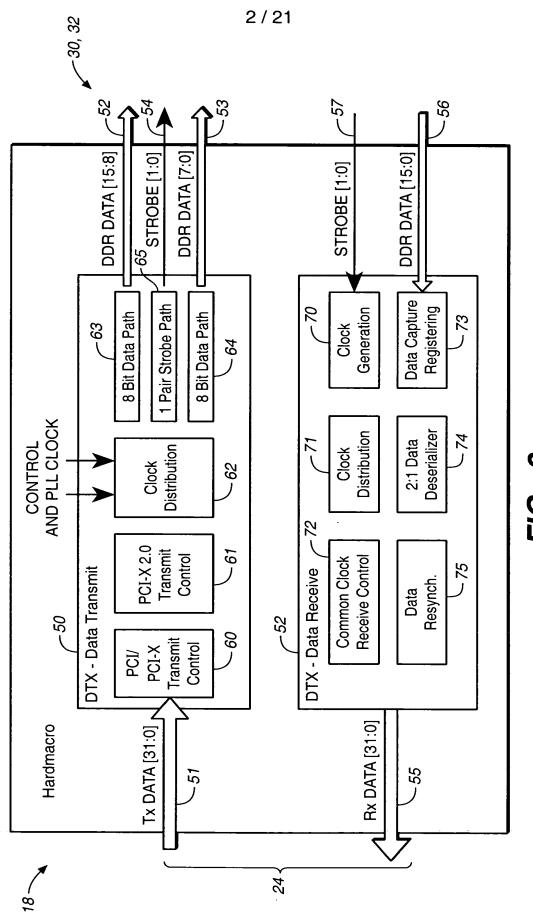
1/21



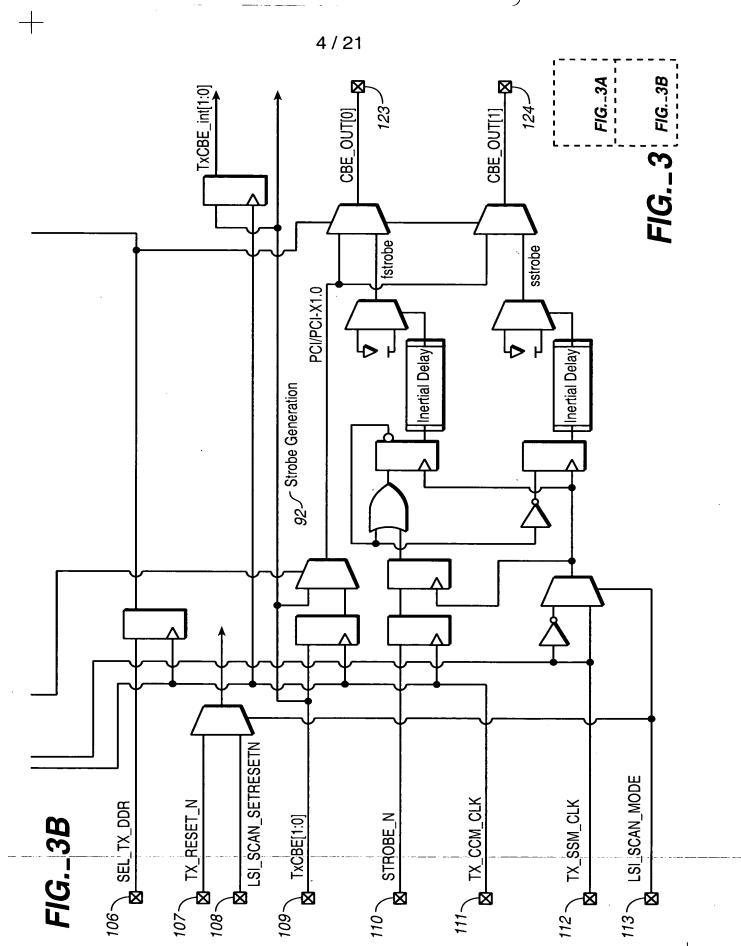
10



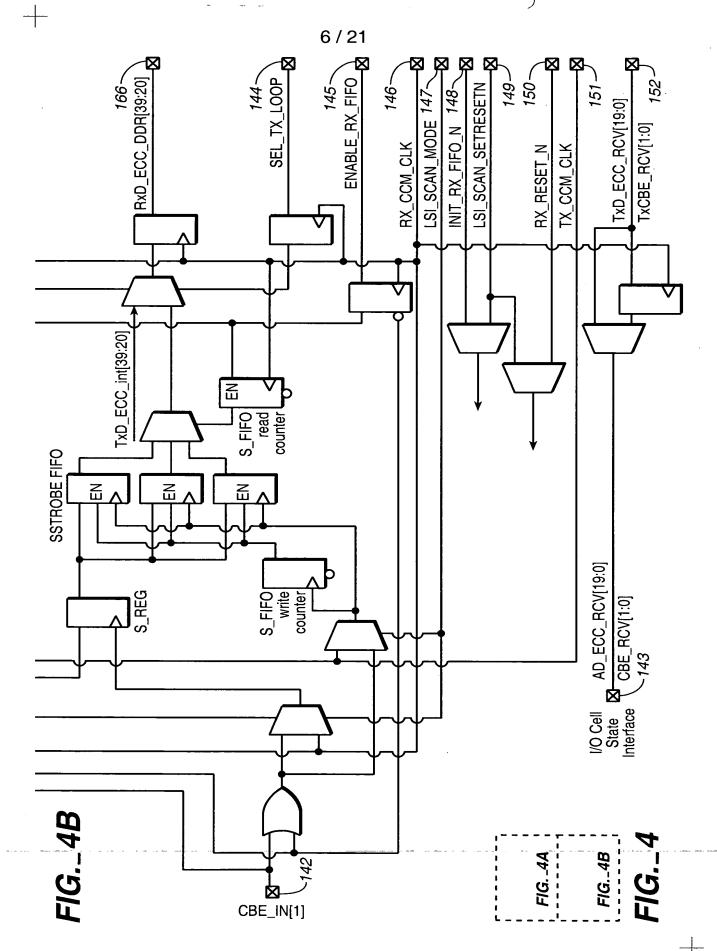
F/G._2

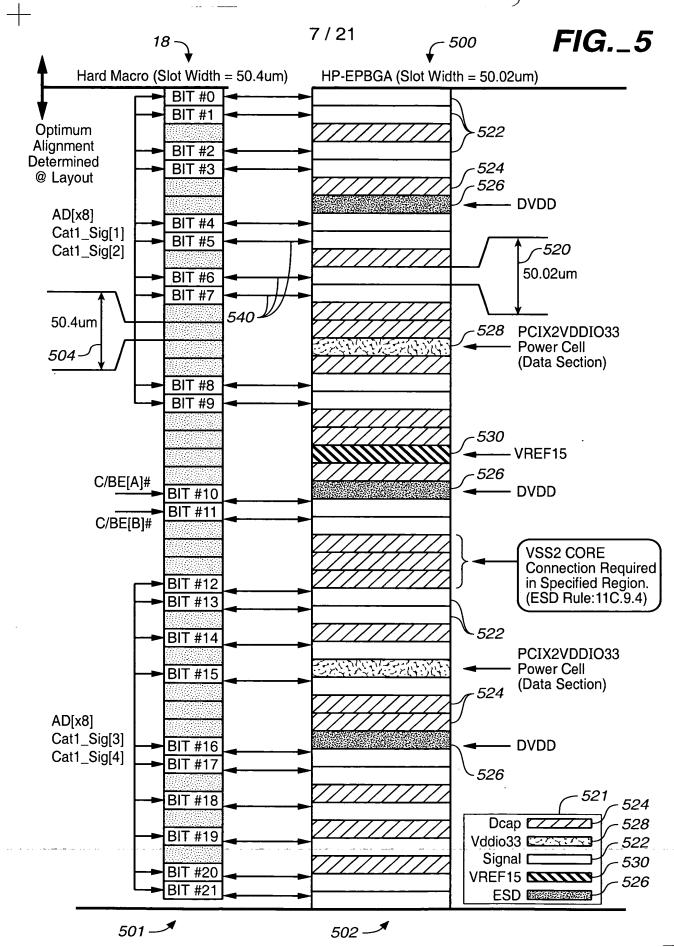
3/21 I/O Cell State Interface I/O Cell Data Interface AD_ECC_TERM[19:0] 121~ TxD_ECC_int[39:20] CBE_TERM[1:0] AD_ECC_EN[19:0] CBE_EN[1:0] TxD_ECC_int[19:0] 122. 125~ 126 127 PCI/PCI-X (SDR) PCI/X2.0 (DDR) 9 I/O Driver State Control 91 / Multiplexing & DDR Generation nertial Delay Hold Delay Ring Counter 50 ~ TxD_ECC_EN[19:0]
TxD_ECC_TERM[19:0] TxCBE_EN[1:0]

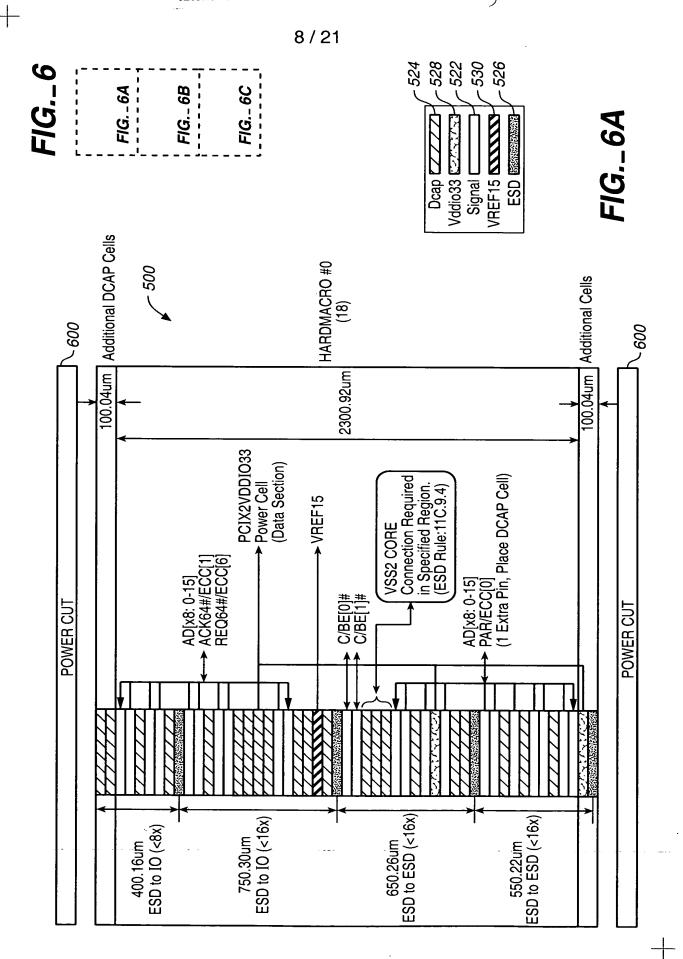
TxCBE_TERM[1:0] TxD_ECC[19:0] SEL_TX_PCI

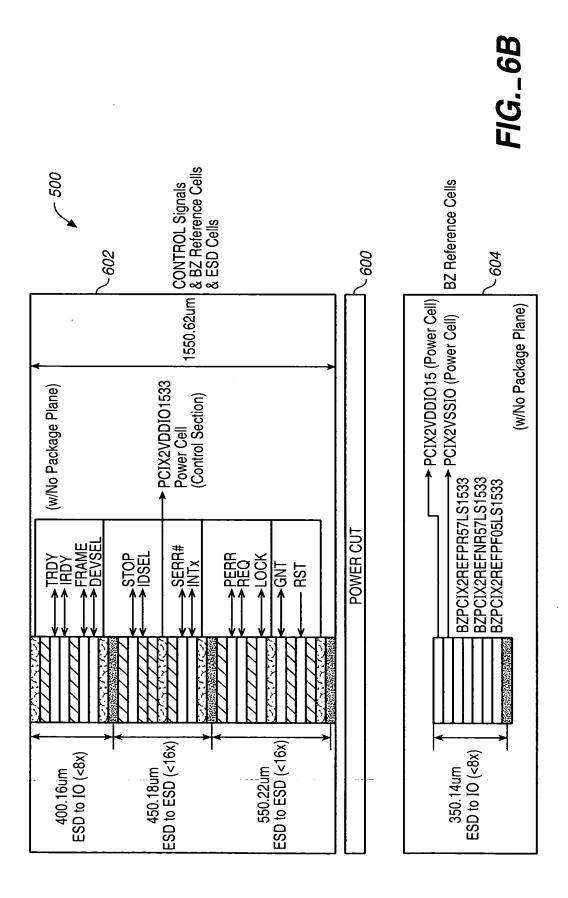


5/21 RxD_ECC_DDR[19:0] *165~* | | RxCBE_DDR[1:0] RXD ECC SDR[19:0] RxD_ECC_PCI[19:0] RxCBE_SDR[1:0] RXCBE PCI[1:0] TxD_ECC[19:0] TxD_ECC_int[19:0] PCI-X1.0 (SDR) \overline{S} PCI-X2.0 (DDR) $\frac{1}{2}$ TxCBEint[1:0] TxCBE[1:0] E F_F| read counter **FSTROBE FIFO** E E 品 F_FIFO counter AC_ECC_IN[19:0] CBE_IN[0] I/O Cell Data Interface

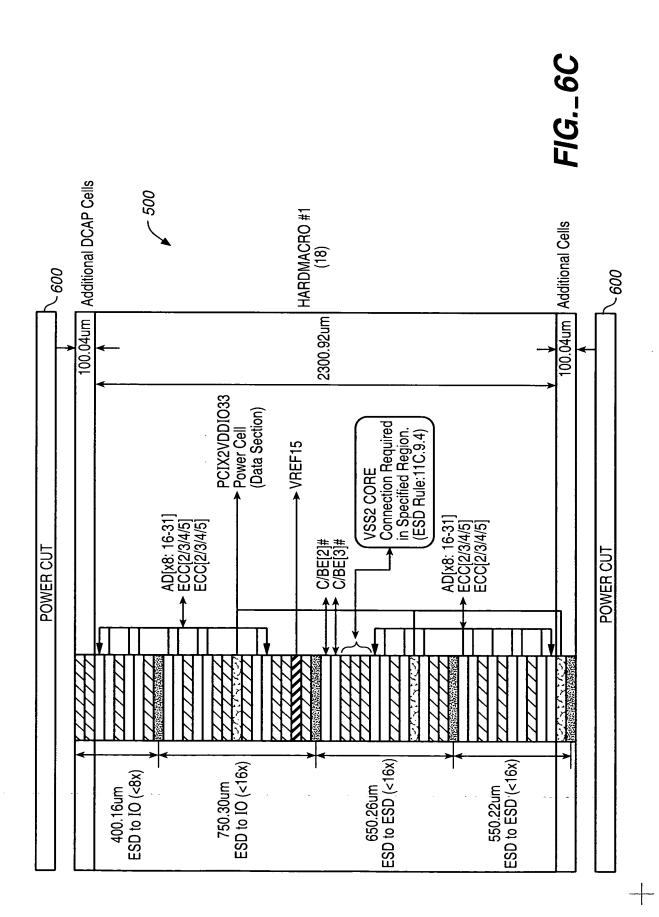


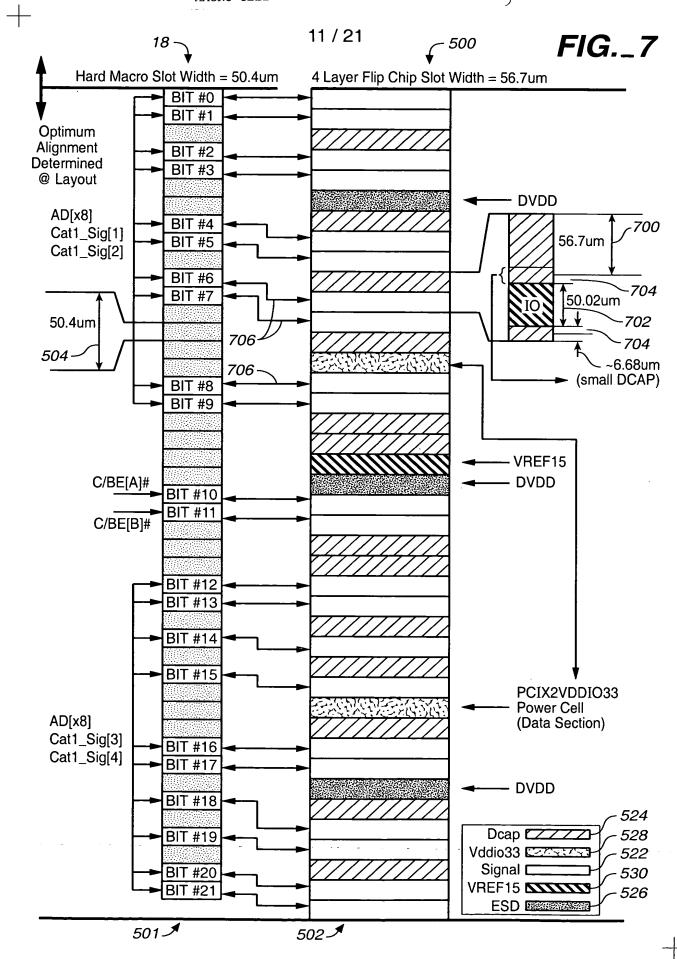






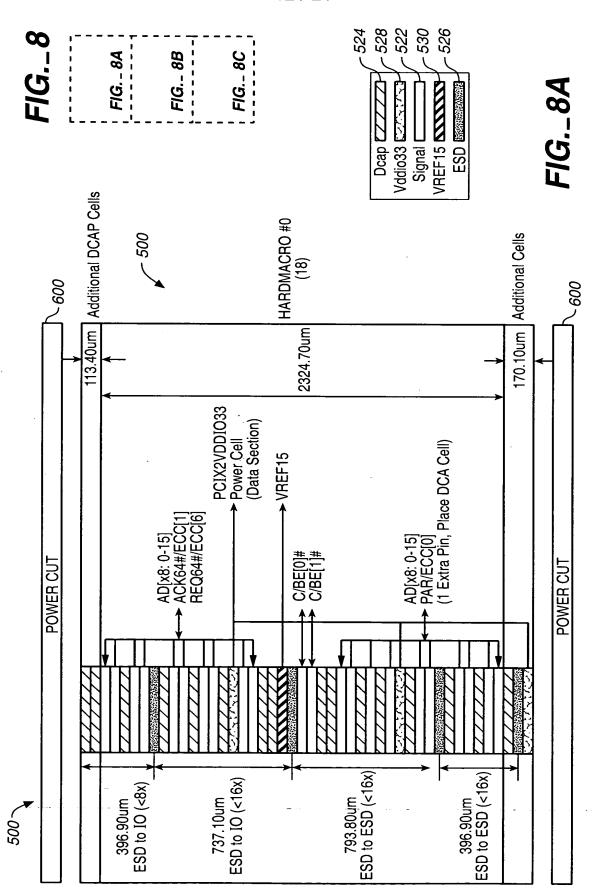
10/21



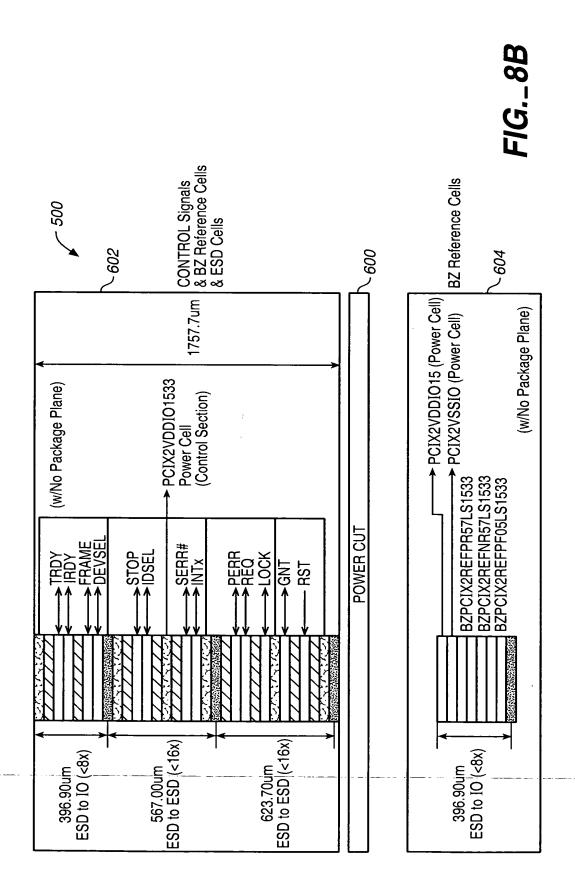


12/21

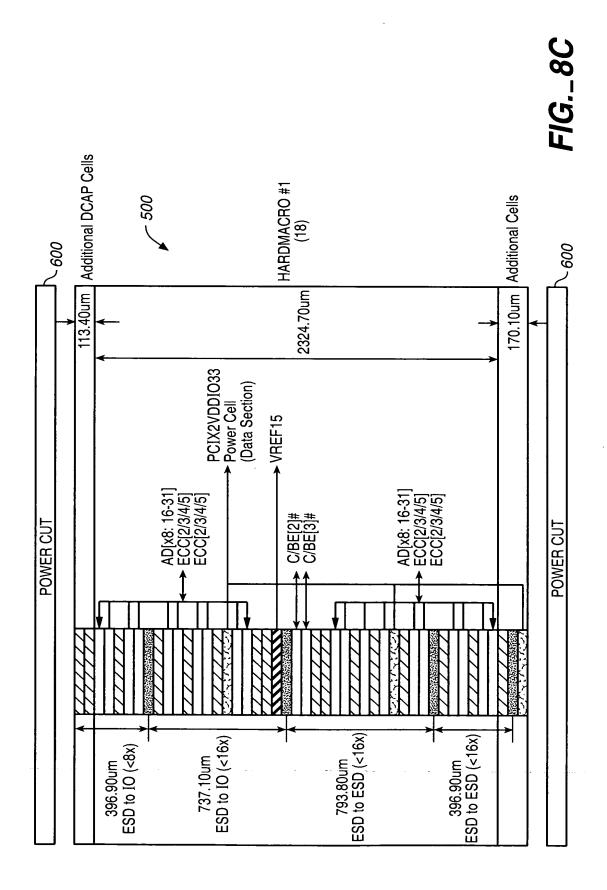
+

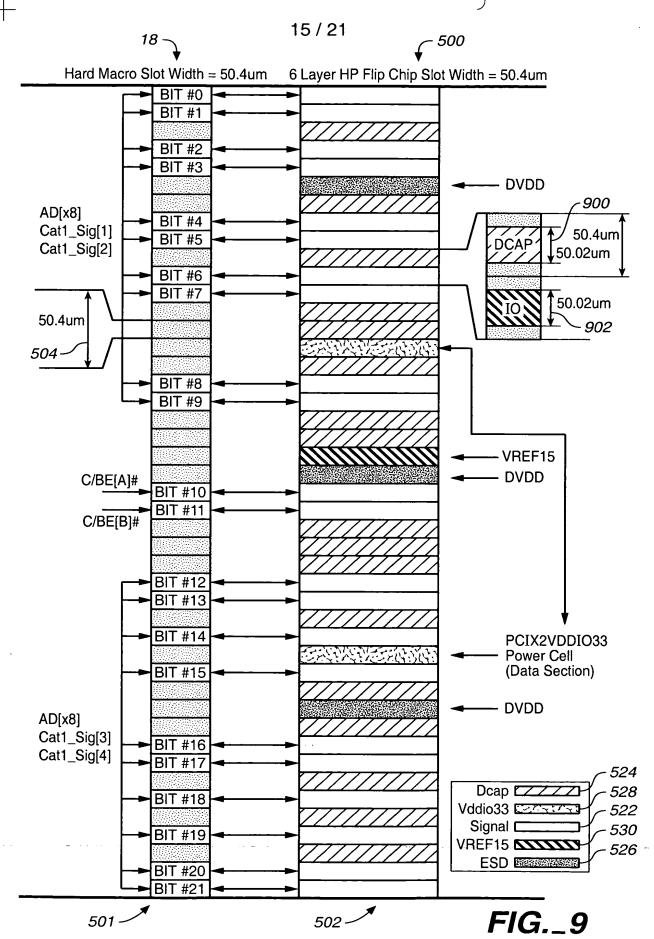


13/21

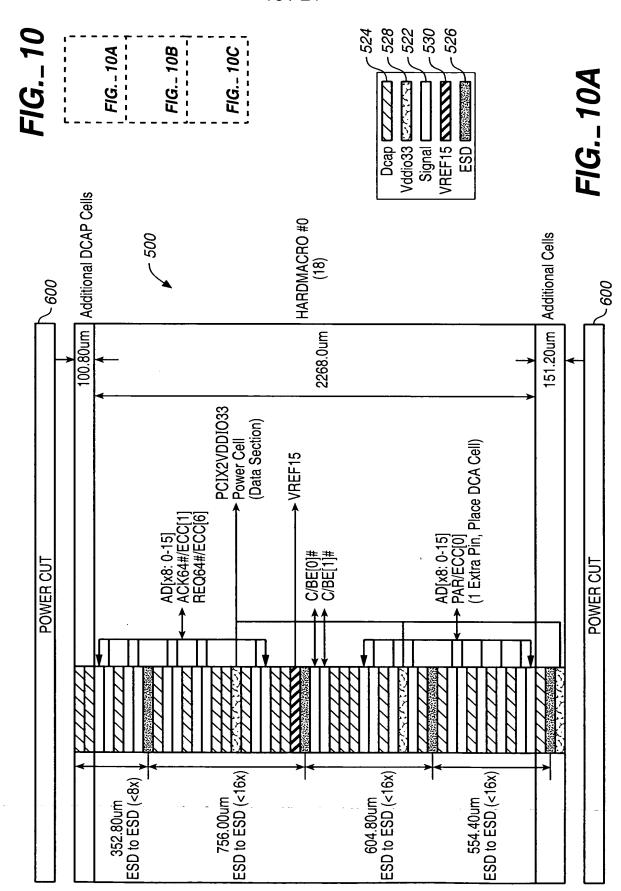


14/21

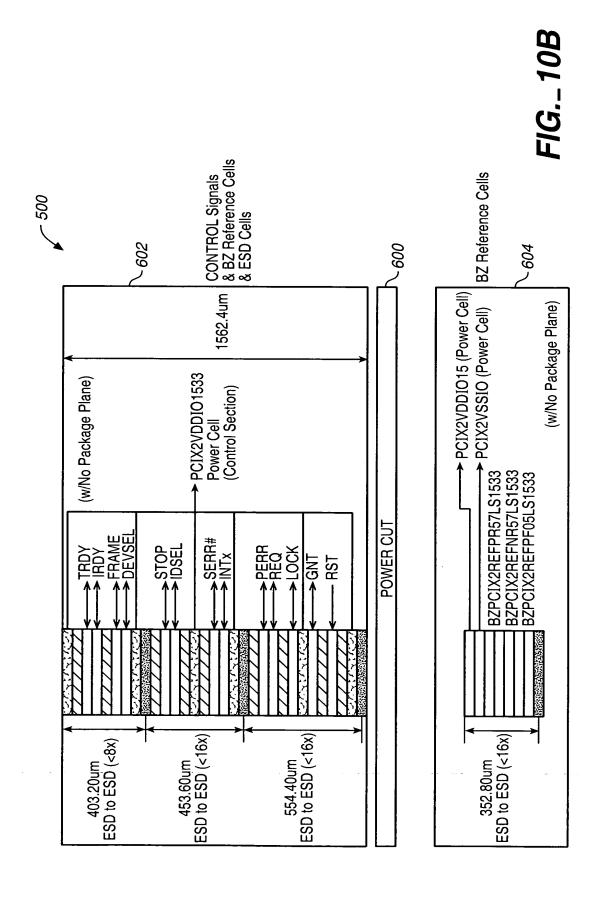




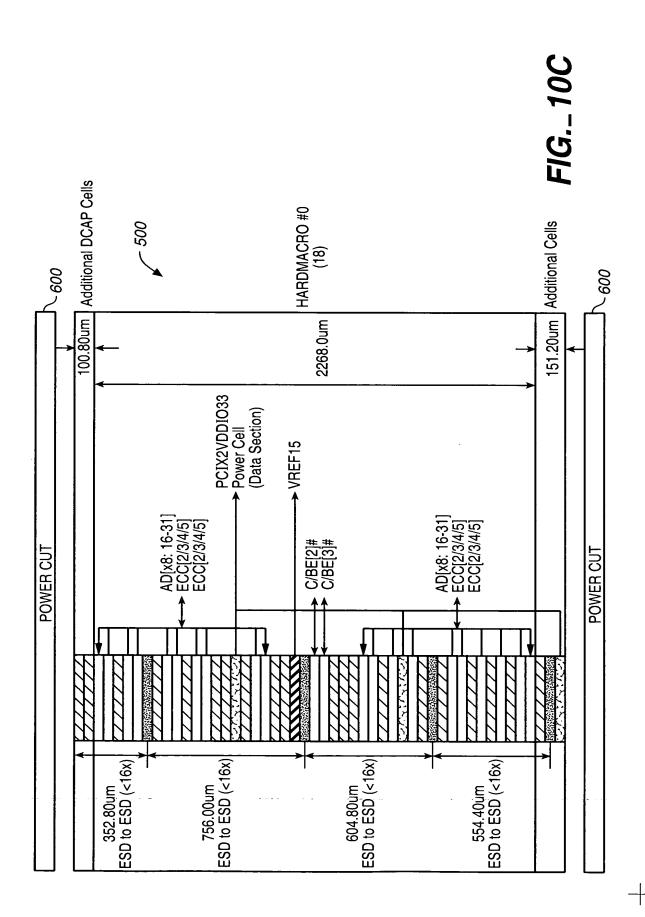
16/21



17/21

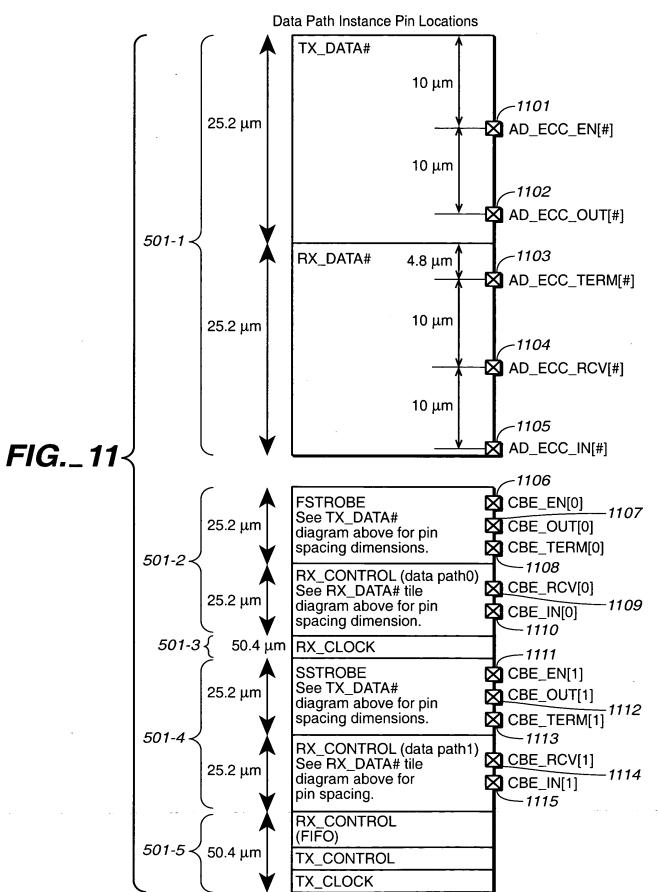


18/21



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20 / 21

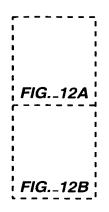


FIG._12

FIG._ 12A

Top Level Floor Plan

- 1200

LSI_SCAN_IN[2:0]

Data path instance pins:

TxD_ECC_EN[#] TxD_ECC_TERM[#] TxD_ECC_RCV[#]

RxD_ECC_PCI[#] TxD_ECC[#] RxD_ECC_DDR[#] RxD_ECC_SDR[#] TxD_ECC[#] RxD_ECC_DDR[#] Scan input routing

TX_DATA0

RX_DATA0

AD_ECC_EN[0]

AD_ECC_OUT[0]
AD_ECC_TERM[0] AD_ECC_RCV[0]

AD_ECC_IN[0]

21/21

Control and aloah	TX_DATA9	AD_ECC_EN[9] AD_ECC_OUT[9] AD_ECC_TERM[9]
Control and clock instance pins:	RX_DATA9	AD_ECC_TEAM[9] AD_ECC_RCV[9] AD_ECC_IN[9]
TxCBE_EN[#] TxCBE_TERM[#] TxCBE_RCV[#]	FSTROBE	CBEEN[0] CBEOUT[0] CBETERM[0]
RxCBE_PCI[#] TxCBE[#]	RX_CONTROL (data path0)	CBERCV[0] CBEIN[0]
RxCBE_DDR[#] RxCBE_SDR[#]	RX_CLOCK	
STROBE_N SEL_TX_LOOP ENABLE_RX_FIFO	SSTROBE	CBE_EN[1] CBE_OUT[1]
SEL_TX_DDR SEL_TX_PCI	RX_CONTROL (data path1)	CBETERM[1] CBERCV[1] CBEIN[1]
LSI_SCAN_MODE LSI_SCAN_SETRESETIN TX_RESET_N	RX_CONTROL (FIFO)	
TX_CCM_CLK TX_SSM_CLK LSI_SCAN_ENABLE	TX_CONTROL	
RX_RESET_N INIT_RX_FIFO_N RX_CCM_CLK	TX_CLOCK	
	TX_DATA10	AD_ECC_EN[10] AD_ECC_OUT[10] AD_ECC_TERM[10]
Data path instance pins:	RX_DATA10	AD_ECC_RCV[10] AD_ECC_IN[10]
TxD_ECC_EN[#] TxD_ECC_TERM[#] TxD_ECC_RCV[#]	•	
RxD_ECC_PCI[#] TxD_ECC[#] RxD_ECC_DDR[#]	•	
RxD_ECC_SDR[#] TxD_ECC[#] RxD_ECC_DDR[#]	TX_DATA19	AD_ECC_EN[19] AD_ECC_OUT[19] AD_ECC_TERM[19]
	RX_DATA19	AD_ECC_RCV[19] AD_ECC_IN[19]
LSI_SCAN_OUT[2:0] LSI_SCAN_OUT_LD[2:0]	Scan output routing	

FIG._12B